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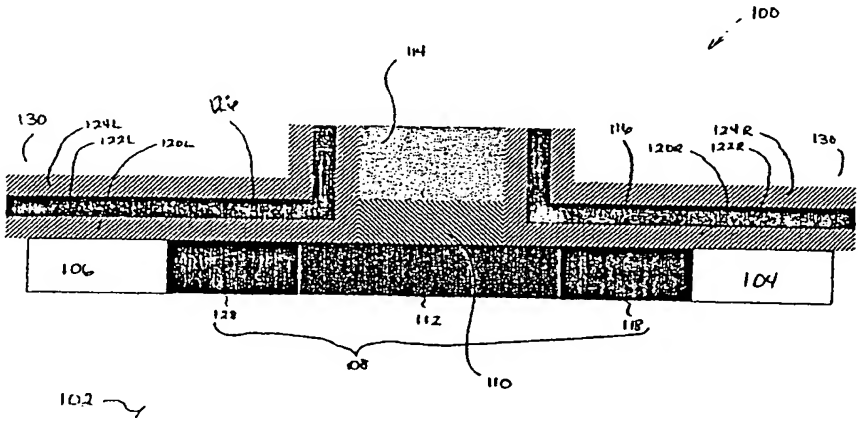
(54) Title: NON-VOLATILE MEMORY STRUCTURE FOR TWIN-BIT STORAGE AND METHODS OF MAKING SAME



(57) Abstract: The present application discloses a single cell non-volatile semiconductor memory device for storing two-bits of information. The device has a semiconductor substrate of one conductivity type and right and left diffusion regions formed in the semiconductor substrate of the opposite conductivity type. A channel region is formed between the left and right diffusions regions. A control gate having a thin gate oxide film is formed over a center channel portion of the channel region. A right charge storage region is formed over a right portion of the channel region between the center channel portion and the right diffusion region. A left charge storage region is formed over a left portion of the channel region between the center channel portion and the left diffusion region. Both of the right and left charge storage regions having a thin oxide layer on the semiconductor substrate, a nitride layer on the thin oxide layer and an insulating oxide layer on the nitride layer. Each of the right and left charge storage regions are capable of storing one-bit of information, which can be programmed and read through minimal adaptation of standard EPROM techniques. Various methods of fabricating this novel cell are also disclosed.

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NON-VOLATILE MEMORY STRUCTURE FOR TWIN-BIT STORAGE AND METHODS OF MAKING SAME

Background of the Invention

1. Field of the Invention

The present invention relates in general to non-volatile digital memories and, more particularly, to an improved cell structure for a programmable non-volatile memory (such as conventional EEPROM or Flash EEPROM) that stores two-bits of information and methods for fabricating same.

2. Background Art

Non-volatile memory devices, such as EPROM, EEPROM, and flash EPROM devices, generally include a matrix of transistors which act as memory cells for storing a single-bit of information. Each transistor in this matrix has source and drain regions formed on a n- or p-type semiconductor substrate, a thin tunnel dielectric layer formed on the surface of the semiconductor substrate positioned at least between the source and drain regions, a floating gate (formed of polysilicon) positioned on the insulating layer for holding a charge, a control gate and an interpoly dielectric positioned between the floating gate and control gate.

Traditionally, the interpoly dielectric had consisted of a single layer of silicon dioxide (SiO_2). However, more recently oxide/nitride/oxide composites (sometimes referred to as an ONO structure) have been used in place of the silicon dioxide because they exhibit decreased charge leakage over the single oxide layer (see Chang et al. U.S. Patent No. 5,619,052).

U.S. Patent No. 5,768,192 to Eitan discloses that ONO structures (as well as other charge trapping dielectrics) have been used as both insulator and floating gate. Fig. 1 shows the prior art structure disclosed in Eitan. Eitan teaches that by programming and reading this transistor device in opposite directions (i.e. reversing "source" and "drain") shorter programming times still result in a high increase in exhibited threshold voltage. Eitan suggests that this result is useful in reducing programming time while still preventing

"punch through" (i.e. a condition where the lateral electric field is strong enough to draw electrons through to the drain, regardless of the applied threshold level).

The semiconductor memory industry has been researching various techniques and approaches to lower the bit cost of non-volatile memory. Two of the more important approaches are dimensional shrinking and multilevel storage. Multilevel storage (often referred to as multilevel cells) means that a single cell can represent more than one bit of data. In conventional memory cell design, only one bit has been represented by two different voltage levels, such as 0V and 5V (in association with some voltage margin), which represent 0 or 1. In multilevel storage more voltage ranges/current ranges are necessary to encode the multiple bits of data. The multiple ranges lead to reduced margins between ranges and require advanced design techniques. As a result, multilevel storage cells are difficult to design and manufacture. Some exhibit poor reliability. Some have slower read times than convention single-bit cells.

Accordingly, it is an object of the present invention to produce a non-volatile memory structure that achieves cost-savings by providing a structure capable of storing two bits of data, thus doubling the size of the non-volatile memory. It is an associated object of the present invention for this cell structure to operate without the use of reduced margins or advanced design techniques.

These and other objects will be apparent to those of ordinary skill in the art having the present drawings, specification and claims before them.

Summary of the Invention

The present application discloses a single cell non-volatile semiconductor memory device for storing two-bits of information. The device has a semiconductor substrate of one conductivity type and right and left diffusion regions formed in the semiconductor substrate of the opposite conductivity type. A channel region is formed between the left and right diffusion regions. A control gate having a thin gate oxide film is formed over a center channel portion of the channel region. A right charge storage region is formed over a right portion of the channel region between the center channel portion and the right diffusion region. A left charge storage region is formed over a left portion of the channel region between the center channel portion and the left diffusion region. Both of the right

and left charge storage regions having a thin oxide layer on the semiconductor substrate, a nitride layer on the thin oxide layer and an insulating oxide layer on the nitride layer. Each of the right and left charge storage regions are capable of storing one-bit of information, which can be programmed and read through minimal adaptation of standard EPROM techniques.

This cell can be fabricated by (1) forming a thin oxide layer on a semiconductor substrate of one conductivity type; (2) depositing a polysilicon control gate on a select portion of the thin oxide layer, thus leaving exposed portions of the thin oxide layer; (3) forming an ONON structure on top of the polysilicon control gate and exposed portions of the thin oxide layer; (4) implanting ions in the semiconductor substrate under the exposed portions of the thin oxide to form right and left diffusion regions of the same conductivity type in the semiconductor substrate; (5) depositing a spin-of-glass layer over the exposed portions of the thin oxide; (6) etching the ONON structure from the top of the polysilicon control gate; (7) remove the spin-of-glass layers; (8) remove the top nitride layer from the ONON structure; and (9) depositing a polysilicon wordline layer over the entire structure.

In another method of fabricating the novel memory cell of the present invention by (1) forming an ONO structure on top of a semiconductor substrate; (2) deposing an oxide strip on a portion of the ONO structure; (3) forming polysilicon spacers adjacent to both sides of the oxide strip; (4) implanting ions in the semiconductor substrate under the portions of the semiconductor substrate not covered by the oxide strip and adjacent polysilicon spacers; (5) removing the oxide strip and exposed portions of oxide layer of the ONO structure; (6) etching the exposed portions of the nitride layer; (7) removing the polysilicon spacers; and (8) deposing a polysilicon line on the bottom oxide of the ONO structure over the entire semiconductor memory device.

Brief Description of the Drawings

Fig. 1 of the drawings is a cross-sectional view -- taken along the wordline -- of the twin-bit non-volatile memory cell according to the present invention;

Figs. 2A and 2B of the drawings are cross-sectional views – taken along the wordline – depicting electron flow in programming and reading each of bits in the twin-bit non-volatile memory cell according to the present invention;

Fig. 3 of the drawings a graphical depiction of the effect of reversing the directionality of the program and read steps on the threshold voltages exhibited by the twin-bit non-volatile cell structure of the present invention;

Figs. 3A through 3H of the drawings are cross-sectional views – taken along the wordline – of the various steps taken in a first method for fabricating a twin-bit non-volatile memory cell according to the present invention;

Figs. 4A through 4H of the drawings are cross-sectional views – taken along the wordline – of the various steps taken in a second method for fabricating a twin-bit non-volatile memory cell according to the present invention; and

Figs 5A through 5J of the drawings are cross-sectional views – taken along the wordline – of the various steps taken in a third method for fabricating a twin-bit non-volatile memory cell according to the present invention.

Best Modes of Carrying Out the Invention

While the present invention may be embodied in many different forms and produced by various different fabrication processes, there is shown in the drawings and discussed herein one specific embodiment and three specific fabrication methods with the understanding that the present disclosure is to be considered only as an exemplification of the principles of the invention and is not intended to limit the invention to the embodiments illustrated.

Fig. 1 shows the twin-bit non-volatile memory structure 100 according to the present invention. Memory structure 100 is based on a semiconductor substrate 102. As known, in the art, semiconductor substrate 102 can be doped to form a p-type or n-type substrate. For purposes of the present explanation of the properties of the present invention, reference shall be made solely to a cell based on a p-type semiconductor substrate. However, as would be understood by those skilled in the art, the present invention is equally applicable to a cell based on an n-type semiconductor substrate with adjustments that would be similarly understood.

Right diffusion region or channel 104 is formed in semiconductor substrate 102 and has a conductivity type opposite to the conductivity type of substrate 102. Left diffusion region or channel 106 is fashioned in semiconductor substrate 102 apart from right

diffusion region 104 thus forming channel region 108 between right and left diffusion regions 104 and 106. Left and right diffusion regions have the same conductivity type (n+ in the disclosed embodiment).

As is known by those of ordinary skill in the art, diffusion regions 104, 106 in a MOS transistor are indistinguishable in a zero-bias state; thus, the role of each diffusion region is defined after terminal voltages are applied with the source biased higher than the drain.

Structure 100 further comprises gate insulating film layer 110 (gate oxide layer) formed on center channel portion 112 of channel region 108. Gate insulating film layer 110 has the thickness necessary to prevent breakdown when high voltage is applied to the control gate electrode. Control gate electrode 114 is a polysilicon layer located on gate oxide layer 110. As detailed below, control gate 114 also functions to insulate the left and right memory "cells" from one another.

Thin (tunneling) oxide layer 120R, nitride layer 122R, and insulating oxide layer 124R are uniformly layered over the right side of control gate electrode 114 and the portion of the semiconductor substrate 102 to the right of control gate 114 (as illustrated in Fig. 1) to form a right ONO dielectric composite layer. In a preferred embodiment, oxide layers 120R and 124R are each approximately 100 micron thick whereas the nitride layer is approximately 50 microns thick. The right dielectric structure forms a right charge storage region 116 on a right portion 118 of channel region 108 between center channel portion 112 and right diffusion region 104.

Thin (tunneling) oxide layer 120L, nitride layer 122L, and insulating oxide layer 124L are uniformly layered over the left side of control gate electrode 114 and the portion of the semiconductor substrate 102 to the left of control gate 114 (as illustrated in Fig. 1) to form a left ONO dielectric composite layer. In a preferred embodiment, oxide layers 120L and 124L are each approximately 100 micron thick whereas the nitride layer is approximately 50 microns thick. The left ONO dielectric composite layer forms a left charge storage region 126 on a left portion 128 of channel region 108 between center channel portion 112 and left diffusion region 106. Right and left regions 116, 126 are capable of storing one-bit of data each.

Although these dielectric structures have been illustrated as being formed by sandwiching a nitride layer between a thin tunneling oxide and insulating oxide, other dielectric structures could be used instead, such as $SiO_2/Al_2O_3/SiO_2$. Similarly, these dielectric structures need not overlie the entire left and right side of structure 100, rather they need only lie on the semiconductor substrate 102 substantially between the edge of their respective diffusion region and control gate 114 (see, e.g., Fig. 4F).

Polysilicon 130 is used as the wordline. Wordline 130 is electrically connected to control gate 114 and is on top of the left and right ONO dielectric composite layers. Consequently, as known in the art, application of a sufficient voltage on wordline 130 induces an n-channel solely in center channel portion 112 of channel region 108.

Cell structure 100 is preferably utilized in a two dimensional array of memory cells. For each row in the array, the cells in each respective row share a common wordline 130-1 through 130-n. With respect to each of the columns, the drains and sources of the cells in each respective column are respectively connected to the drains and sources of the other cells in that column preferably via a pair of buried bit-lines, thus, minimizing the metallic connections required. Thus, each cell in the memory array can be addressed via wordline 130 by simultaneous selection and appropriate biasing of a particular buried pair of bit-lines for programming, read and erase operations. Thus, addressing the array of cells generally requires standard addressing circuitry. Additionally, though, inasmuch as each cell storage two bits of information, a unique approach to biasing the desired column is required to effect the particularly selected bit from the pair stored within the accessed cell.

Figs. 2A and 2B show the operation/biasing principles of the twin-bit non-volatile memory structure 100 of the present invention. As noted above, in twin-bit non-volatile memory structure 100, one-bit of data can be stored and localized at each of right and left charge storage regions 116 and 126, respectively. As will be explained hereinbelow, by reversing the program and read directions of cell 100, interference between the each of the two charge storage regions can be avoided. Fig. 2A illustrates the programming and reading of the "right bit." To program the right bit, the right diffusion region is treated as the drain (by applying a voltage of 4-6V) and the left diffusion region is treated as the source (by applying 0V or low voltage for hot-e program). To read that right bit, the left diffusion region is treated as drain (by applying a voltage of 1.5-2.5V) and the right

diffusion is treated as the source (by applying a voltage of 0V. As depicted by Fig. 2B, similar operations would be used to program and read the left storage region.

In addition to the modified hot-e programming approach taught above, secondary ion implantation could also be utilized to program cell 100. In that programming approach, the body voltage is lower to approximately –3V while the drain is held at 3 V, the source at 0 V and the gate at 6-10 V. In any event, this novel structure, which presents a thinner oxide layer to the programming currents allows for quicker programming with lower overall voltages.

As shown in Fig. 3 (in which a charge was stored in right charge storage region), the localized trapped electrons exhibit different threshold voltages if read in different directions. The first line depicts the threshold voltage when the right diffusion region is used as drain (the same direction as in the program step). The second line depicts the threshold voltage when the left diffusion is used as drain (the reverse of the program step). As can be seen from these two lines, by reversing the read and program directions used in twin-bit cell structure 100, a more efficient threshold voltage behavior is exhibited. By utilizing this aspect of the design, even though both sides of the cell are programmed to store information, only threshold voltage of single bit is read by selecting either the left or right diffusion region to be the drain.

Erasure of these twin-bit storage cells can be executed by one bit at a time or two bits at a time. If high voltage is applied at both diffusion terminals corresponding with zero or negative gate voltage, the two bits will be erased together. If high voltage is applied at single diffusion terminal, only corresponding with zero or negative gate voltage, only single bit is erased. The over-erase phenomenon is avoided by the cell design because of the central single oxide region. Thus, even if the threshold voltages of storage regions 116 and 126 are over-erased, the effective threshold is still determined by central single oxide region. Consequently, the erased-threshold voltage of the structure is very tight and, thus, suitable for low power applications.

Preferred Methods of Fabrication

There are various possible methods for fabricating the twin-bit cell of the present invention. In particular, three preferred processes have been disclosed hereinbelow with

the understanding that these processes merely exemplify the potential processes by which the twin-bit non-volatile memory structure of the present invention can be fabricated.

First Fabrication Method

A first potential method for fabricating an n-channel version of the twin-bit non-volatile memory structure of Fig. 1 is shown in Figs. 3A through 3H of the drawings. As depicted in Fig. 3A, after threshold voltage adjustment of the semiconductor substrate and formation of gate oxide layer 102 by any of the well-known standard techniques, a bitline mask is used to pattern a series of polysilicon gates 114. Next, as shown in Fig. 3B, ONON (oxide/nitride/oxide/nitride) layers are formed by thermal growth and/or deposition.

Next, self-aligned implantation generates buried N+ diffusion regions for source and drain as shown in Fig.3C. Of course, as would be understood by one skilled in the art, if semiconductor substrate 102 was n-type rather than p-type, P+ diffusion regions would be buried instead.

Then, as shown in Fig. 3D, a Spin of Glass (SiO_2) ("SOG") layer is deposited using conventional techniques (or preferably the technique disclosed in U.S. Patent No. 5,716,673) and etched back to expose the ONON structure on top of the polysilicon forming control gate 114. Thereafter, as shown in Figs. 3E and 3F, the ONON film on top poly are etched and the SOG is removed. Finally, as shown in Figs.3G and 3H, the top nitride layer is removed and a second polysilicon layer 130 is deposited according to the wordline mask. In this manner, polysilicon layer 130 is conductive contact with control gate 114.

Second Fabrication Method

A second potential method for fabricating the twin-bit non-volatile memory structure of Fig. 1 is shown in Figs. 4A through 4H of the drawings. As shown in Fig. 4A, after threshold voltage adjustment of the substrate, ONO (oxide/nitride/oxide) layers are formed on a semiconductor substrate by thermal growth and/or deposition.

Secondly, as shown in Fig. 4B, a bitline mask is used to pattern CVD nitride and then form the poly spacers. Next, self-aligned ion implantation generates buried N+ diffusion regions for source and drain as shown in Fig.4C. Thereafter, the CVD nitride layer is removed (Fig. 4D) and nitride layer outside the spacer region also removed (Fig.

4E). Then, as shown in Figs. 4F and 4G, the poly spacers are removed and the gate oxide is cleaned and may be re-grown for better quality. Finally, as shown in Fig. 4H, a polysilicon line is deposited according to the pattern wordline by wordline mask.

Third Fabrication Method

A third potential method for fabricating the twin-bit non-volatile memory structure of Fig. 1 is shown in Figs. 5A through 5J of the drawings. As shown in Fig. 5A, after threshold voltage adjustment and gate oxide formation, polysilicon layer (poly1) and silicon nitride layer are deposited. First, the bitline mask is used to pattern poly gate (Fig 5A). Secondly, oxide spacers are formed (as shown in fig.5B) by depositing oxide and etching back. Next, self-aligned implantation generates buried N+ diffusion regions for source and drain (Fig.5C). As shown in Figs.5D and 5E, the oxide spacers are removed and ONON (oxide/nitride/oxide/ nitride) layers are formed by thermal growth and deposition. Then, SOG layer is deposited and etched back to expose the ONON films on top of the polysilicon control gate 114 (Fig. 5F). After that, ONON films on control gate 114 are etched (Fig. 5G) and SOG is removed (Fig. 5H). Finally, the top nitride layer is removed (Fig. 5I) and the second polysilicon layer (poly2) deposited and patterned by wordline mask into wordline 130 (Fig. 5J).

Compared to conventional EEPROM or Flash EEPROM, the process of fabricating structure 100 is much simpler because there is no floating gate. Thus, the various difficulties of the prior art related to the floating gate, such as fabrication of the floating gate and insulation between the control and floating gate are avoided. In addition, the over-erase phenomenon is avoided because of the central single oxide region (which exhibits the dominant threshold voltage of the structure) and the inability of the left and right storage regions (which could be "over-erased") to control the entirety of the channel.

The gate coupling ratio ("GCR") of structure 100 is 100%. Consequently, both the program and erase voltages used in combination with this structure can be lower than the program and erase voltages of standard EEPROM or Flash EEPROM cells. As a result of these lower program and erase voltages, smaller pumping effort is required. In addition, these lower voltages release the circuit and process overhead.

A similar consequence of the greatly improved GCR is that the read current of structure 100 is much higher than that of standard EEPROM or Flash EEPROM cells. Thus, higher performance can be achieved with this inventive structure.

Program speed is improved by thinner central single oxide 110 thickness. And the cell is suitable for low power application because of tightened low Vt distribution. Finally, the per bit cost of structure 100 is significantly lower than standard memory due to its double density and the simple processes by which it can be fabricated.

The foregoing description and drawings merely explain and illustrate the invention and the invention is not limited thereto. Those of the skill in the art who have the disclosure before them will be able to make modifications and variations therein without departing from the scope of the present invention.

WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device for storing two-bits of digital information comprising:

- a semiconductor substrate of one conductivity type;

- a right diffusion region formed in said semiconductor substrate, said right diffusion region having a conductivity type opposite to the conductivity type of said semiconductor substrate;

- a left diffusion region formed in said semiconductor substrate apart from said right diffusion region thus forming a channel region between said right and left diffusion regions, said left diffusion region having the same conductivity type as said right diffusion region;

- a gate insulating film formed on a center channel portion of said channel region;

- a control gate electrode formed on said gate insulating film;

- a right charge storage region formed over a right portion of said channel region between said center channel portion and said right diffusion region, said right charge storage region being associated with a right dielectric structure; and

- a left charge storage region formed over a left portion of said channel region between said center channel portion and said left diffusion region, said left charge storage region being associated with a left dielectric structure.

2. The non-volatile semiconductor memory device of Claim 1 wherein said right dielectric structure comprises: a right thin oxide layer on said semiconductor substrate over said right portion of said channel region; a right nitride layer on said right thin oxide layer and a right insulating oxide layer on said right nitride layer.

3. The non-volatile semiconductor memory device of Claim 2 wherein said left dielectric structure comprises: a left thin oxide layer on said semiconductor substrate over said left portion of said channel region; a left nitride layer on said left thin oxide layer and a left insulating oxide layer on said left nitride layer.

4. The non-volatile semiconductor memory device of Claim 1 wherein said right dielectric structure comprises: a right thin oxide layer on said semiconductor substrate over said right portion of said channel region; a right aluminum oxide layer on said right thin oxide layer and a right insulating oxide layer on said right nitride layer.

5. The non-volatile semiconductor memory device of Claim 4 wherein said left dielectric structure comprises: a left thin oxide layer on said semiconductor substrate over said left portion of said channel region; a left aluminum oxide layer on said left thin oxide layer and a left insulating oxide layer on said left nitride layer.

6. A method of fabricating a non-volatile semiconductor memory device for storing two-bits of digital information comprising:

- forming a thin oxide layer on a semiconductor substrate of one conductivity type;

- depositing a polysilicon control gate on a select portion of the thin oxide layer, thus leaving exposed portions of the thin oxide layer;

- forming an ONON structure on top of the polysilicon control gate and exposed portions of the thin oxide layer;

- implanting ions in the semiconductor substrate under the exposed portions of the thin oxide to form right and left diffusion regions of the same conductivity type in the semiconductor substrate;

- depositing a spin-of-glass layer over the exposed portions of the thin oxide;

- etching the ONON structure from the top of the polysilicon control gate;

- remove the spin-of-glass layers;

- remove the top nitride layer from the ONON structure; and

- depositing a polysilicon wordline layer over the entire structure.

7. A method of fabricating a non-volatile semiconductor memory device for storing two-bits of digital information comprising:

- forming an ONO structure on top of a semiconductor substrate;

- deposing an oxide strip on a portion of the ONO structure;

- forming polysilicon spacers adjacent to both sides of the oxide strip;

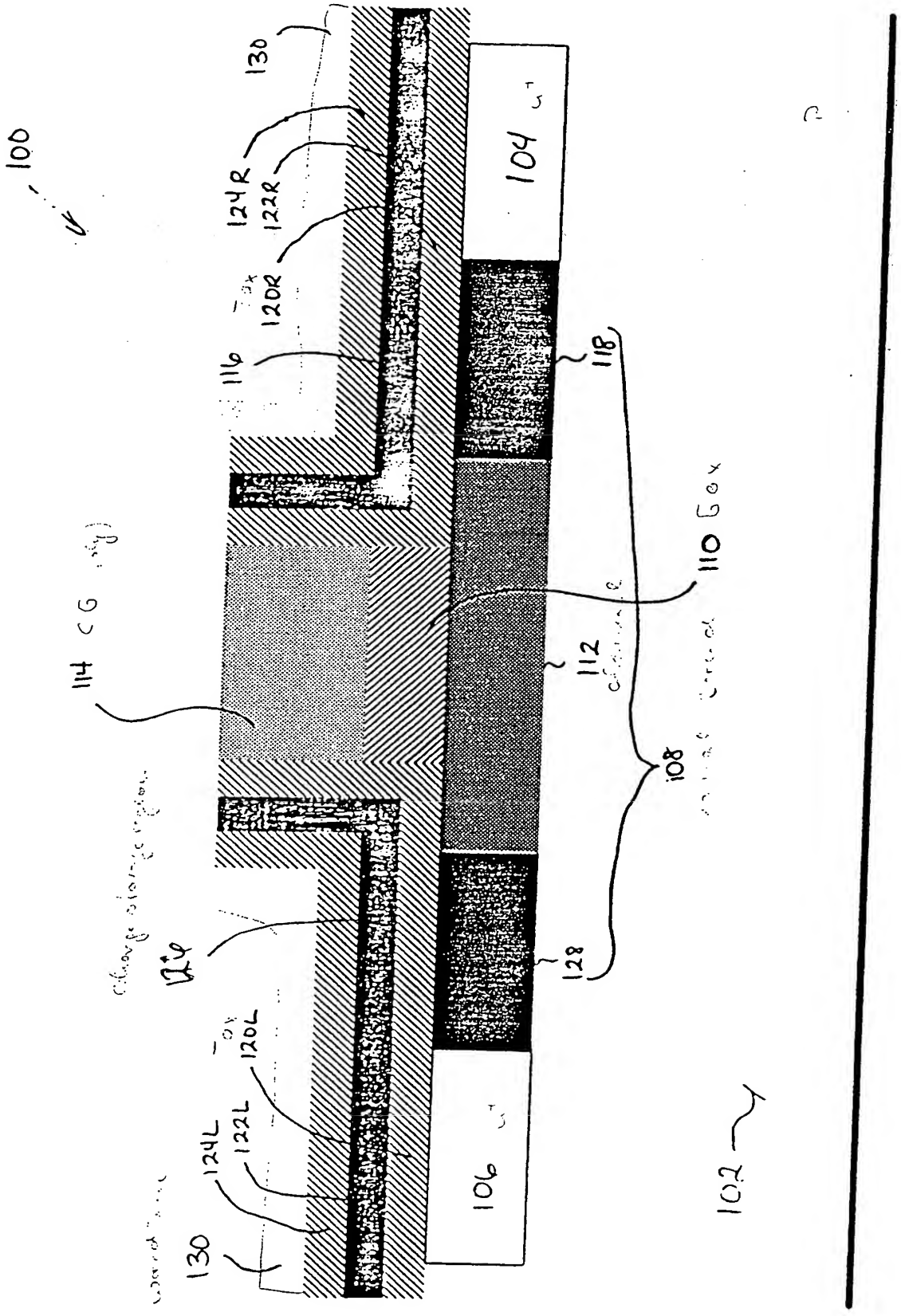
- implanting ions in the semiconductor substrate under the portions of the semiconductor substrate not covered by the oxide strip and adjacent polysilicon spacers;

- removing the oxide strip and exposed portions of oxide layer of the ONO structure;

- etching the exposed portions of the nitride layer;

- removing the polysilicon spacers; and

- deposing a polysilicon line on the bottom oxide of the ONO structure over the entire semiconductor memory device.


100
130
124R
122R
120R
116
104
118
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112
108
114
128
124L
122L
120L
130
106
102

Fig. 1

Fig. 2A

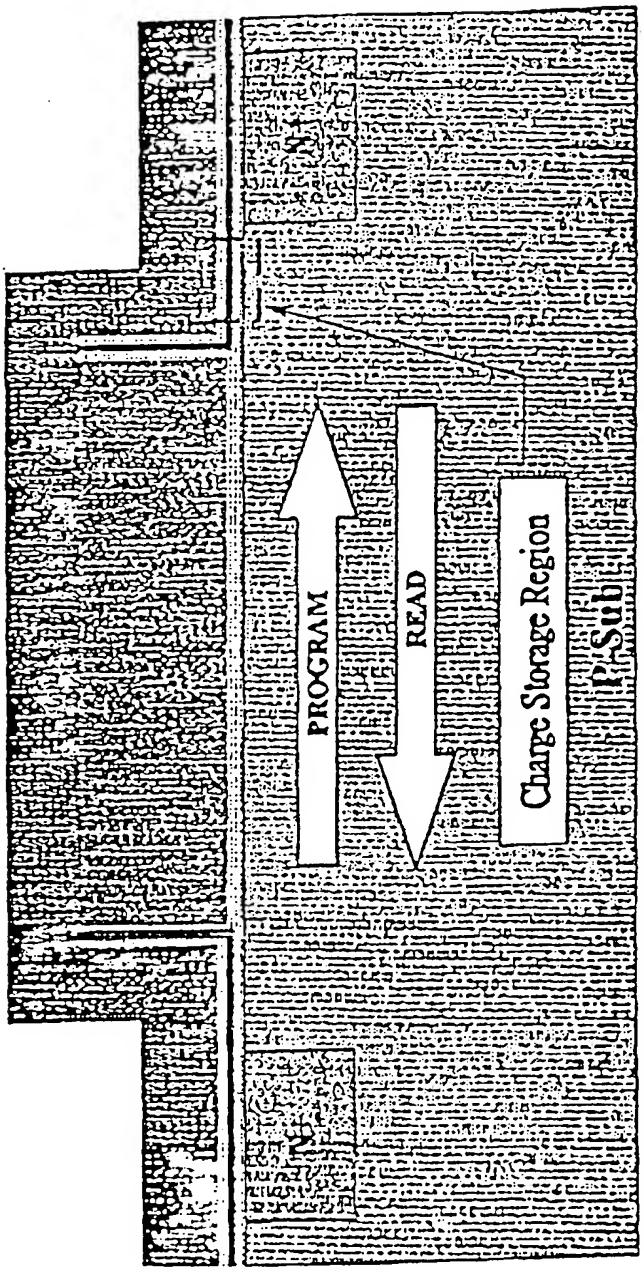
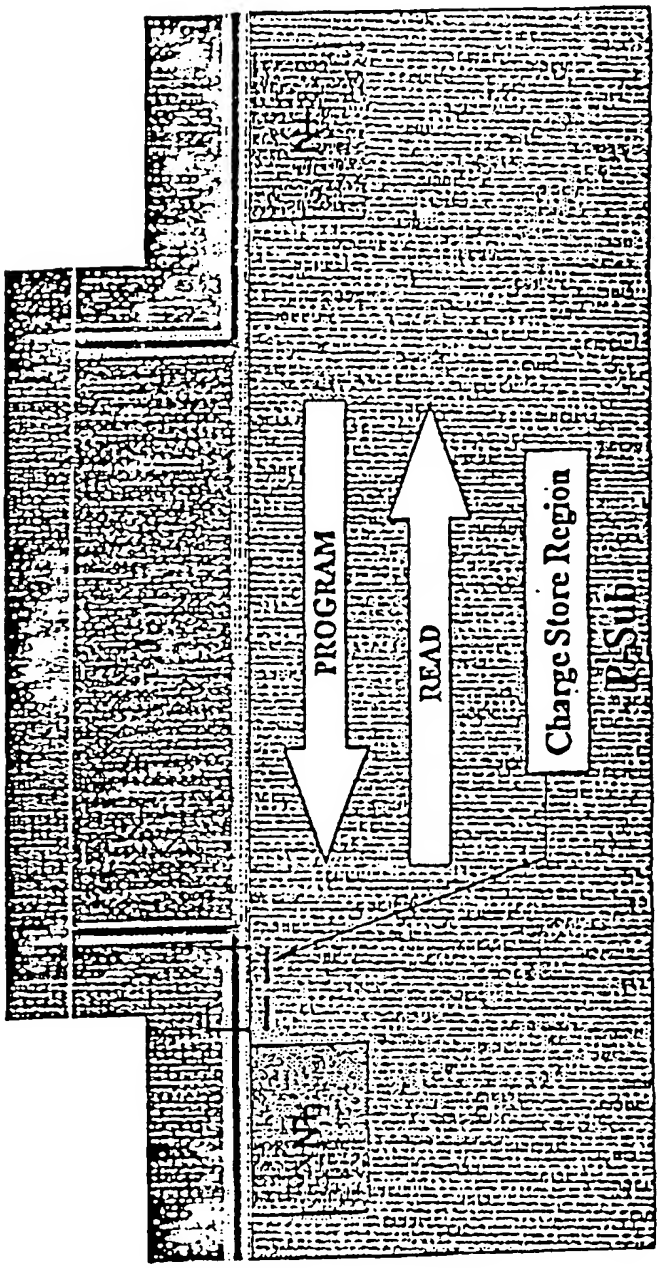


Fig. 2B



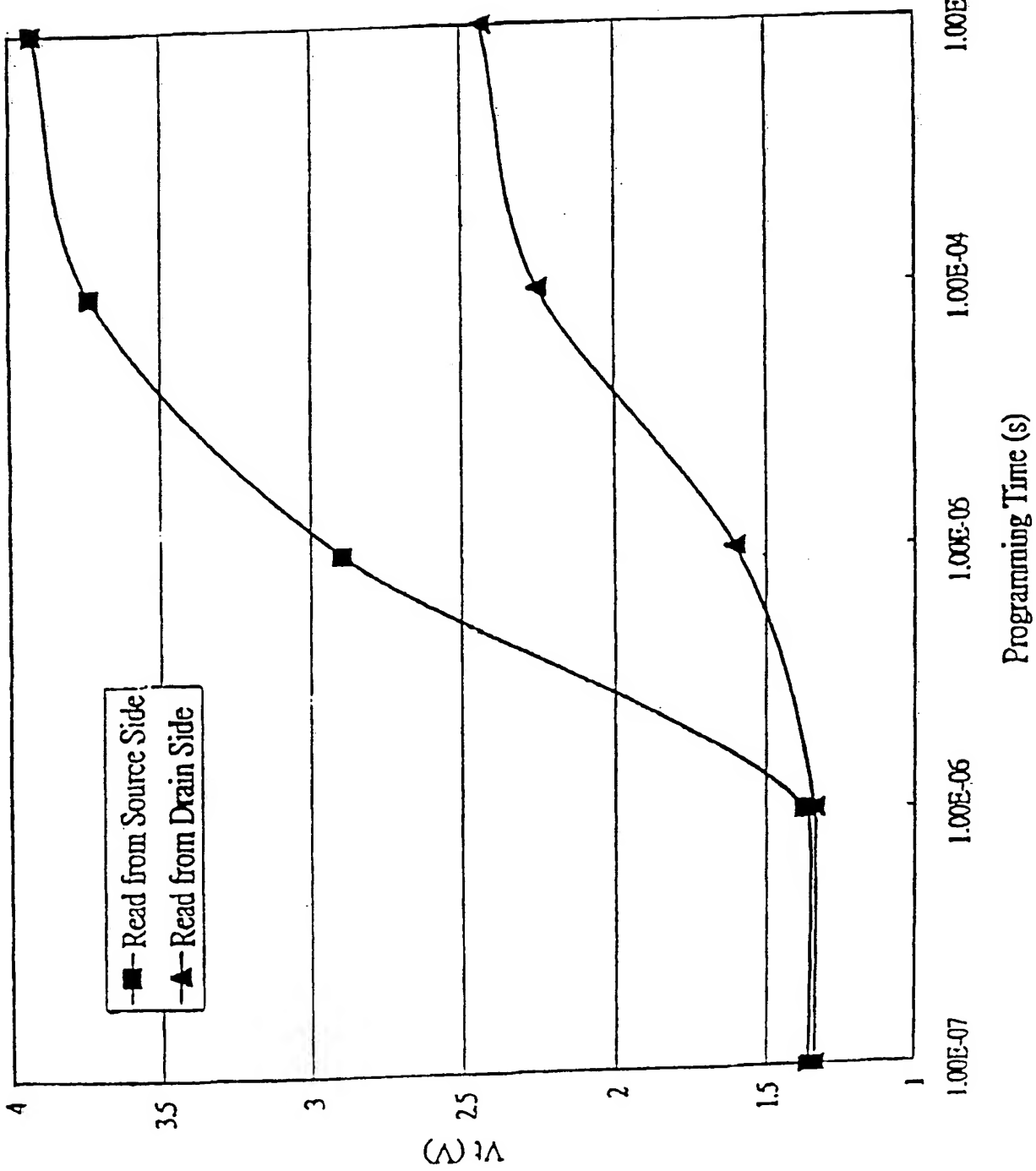

Vt (V)
4
3.5
3
2.5
2
1.5
1
1.00E-07
1.00E-06
1.00E-05
1.00E-04
1.00E-03
Programming Time (s)
Read from Source Side
Read from Drain Side

Fig. 3

Fig. 3A

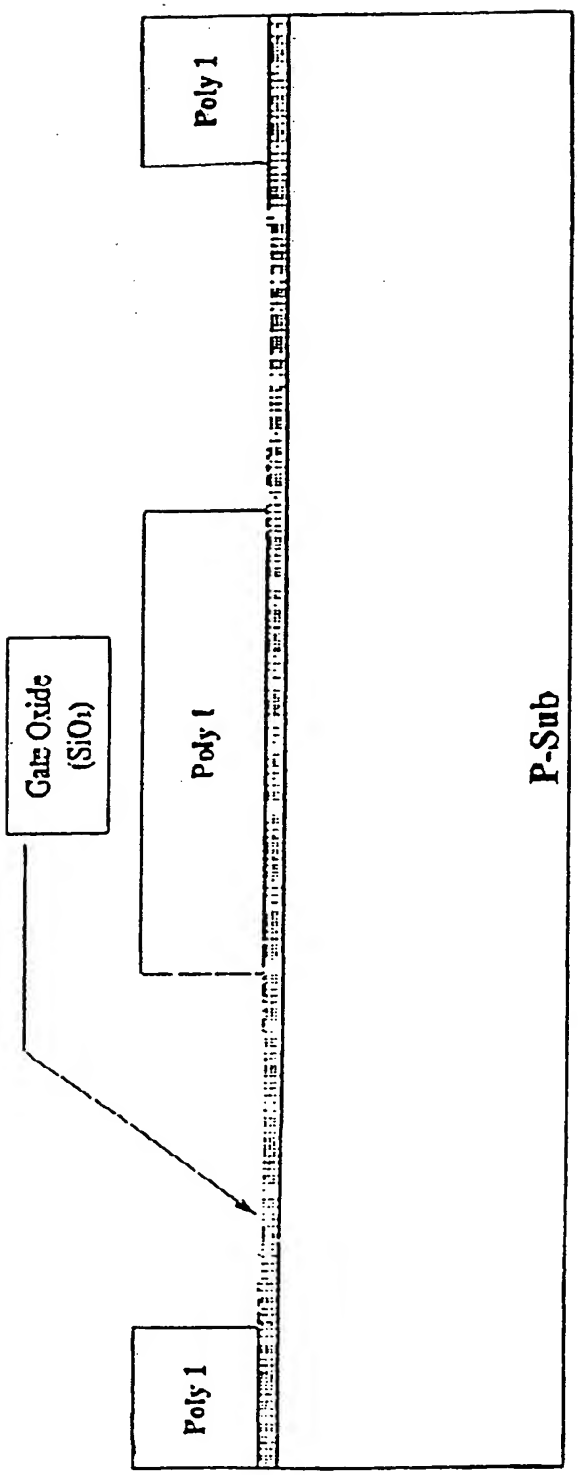


Fig. 3B

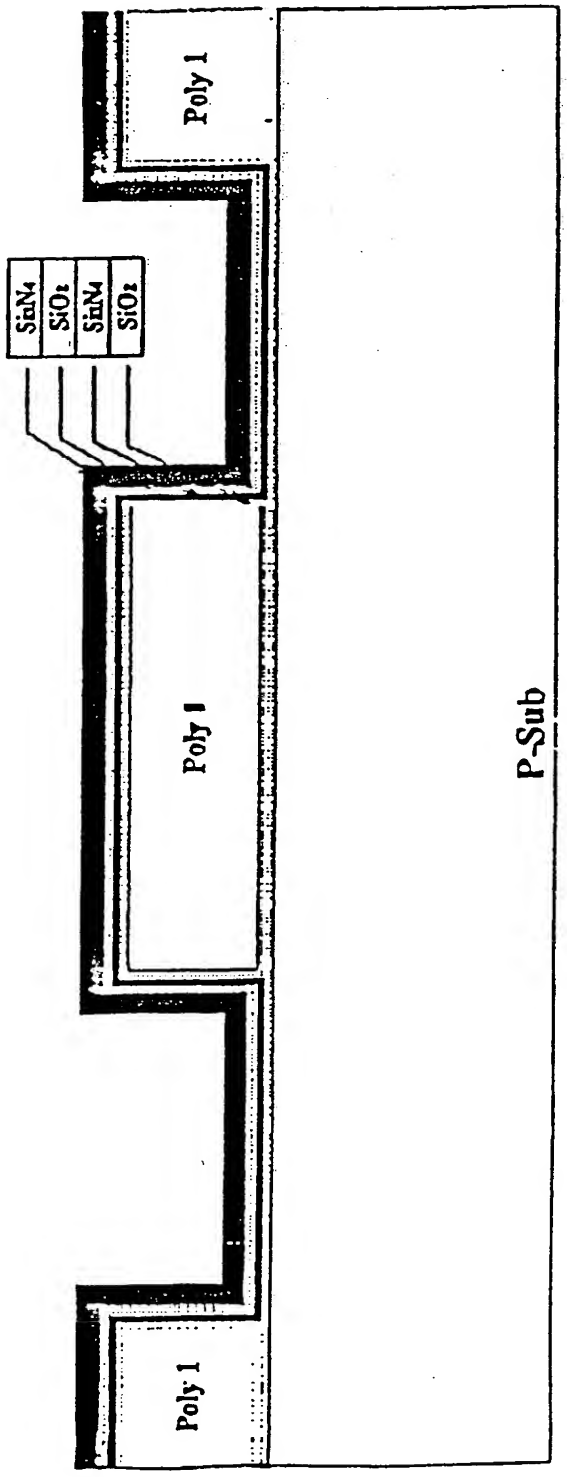


Fig. 3C

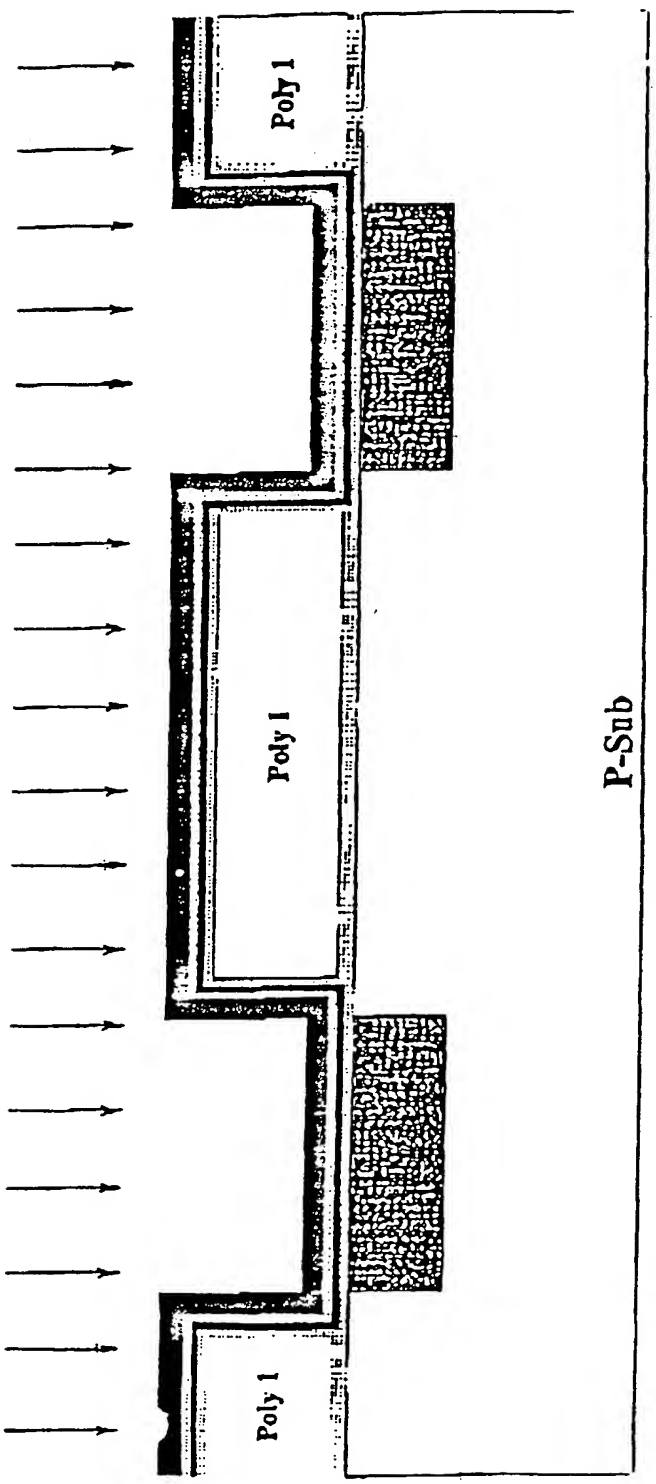


Fig. 3D

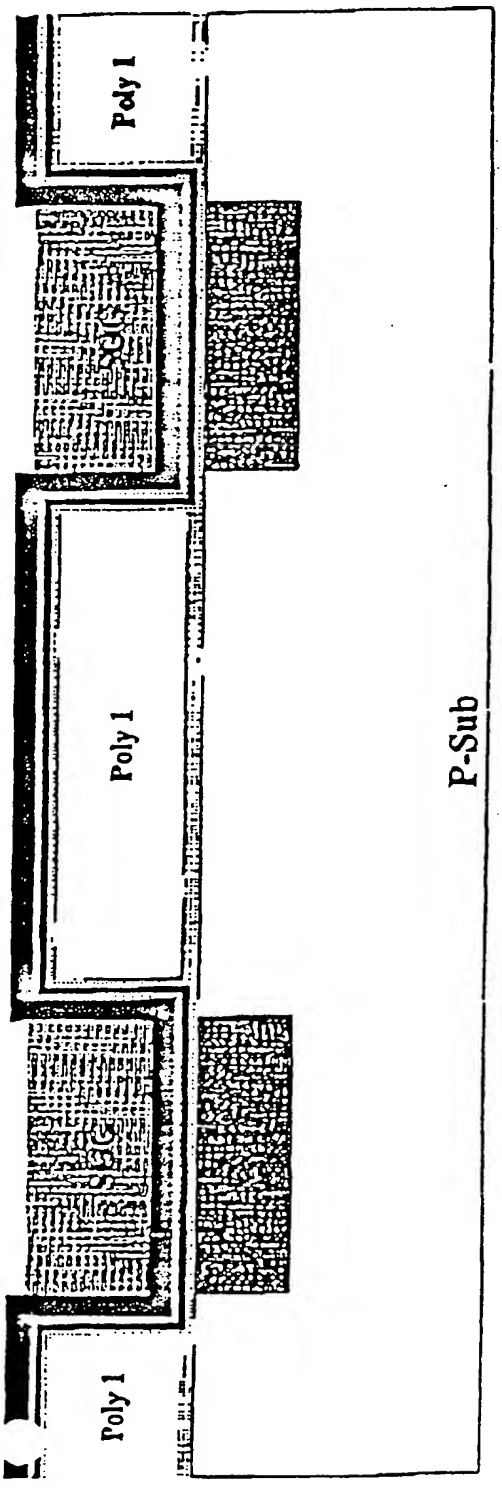


Fig. 3E

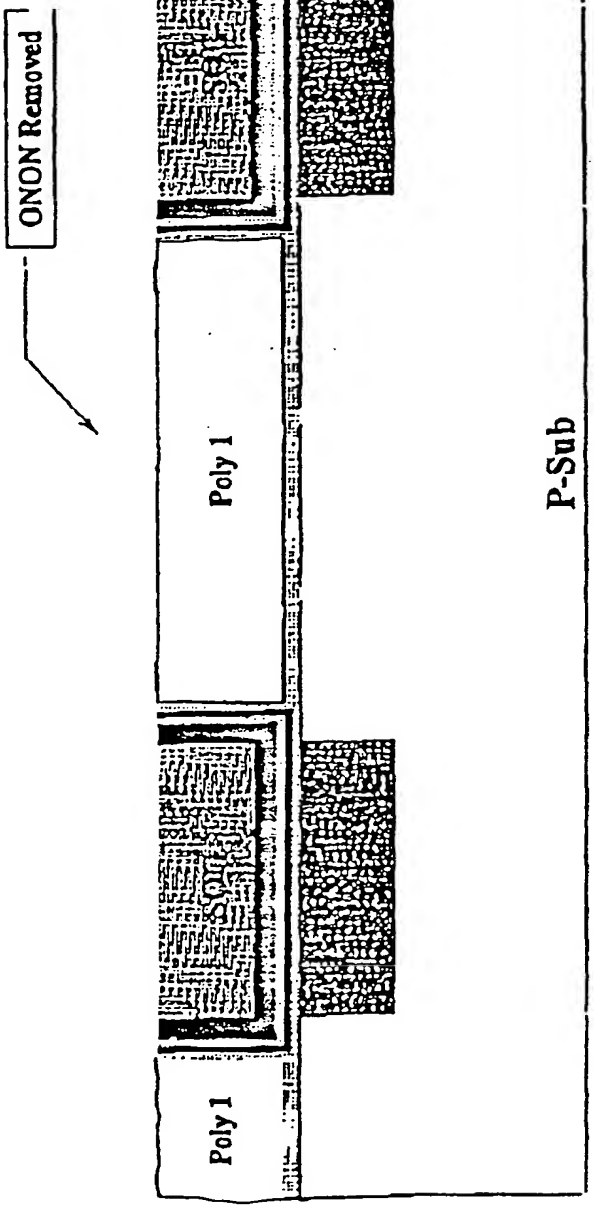


Fig. 3F

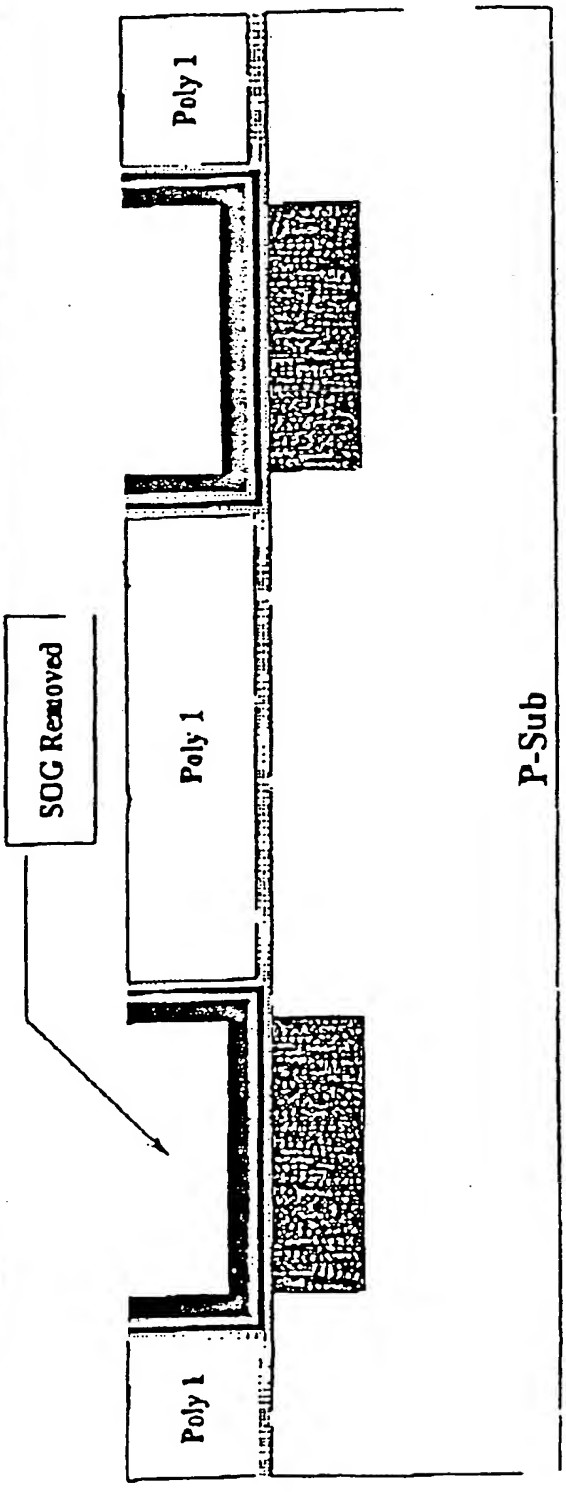
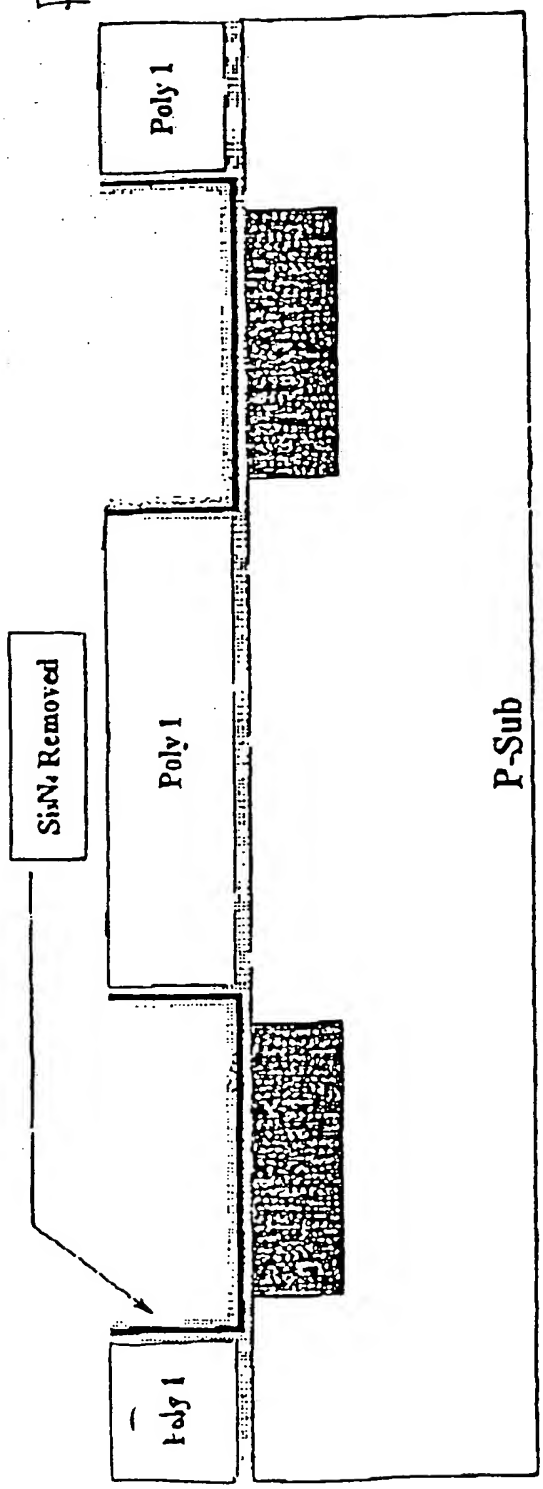


Fig. 3G



POLY 2 Deposition

Fig. 3H

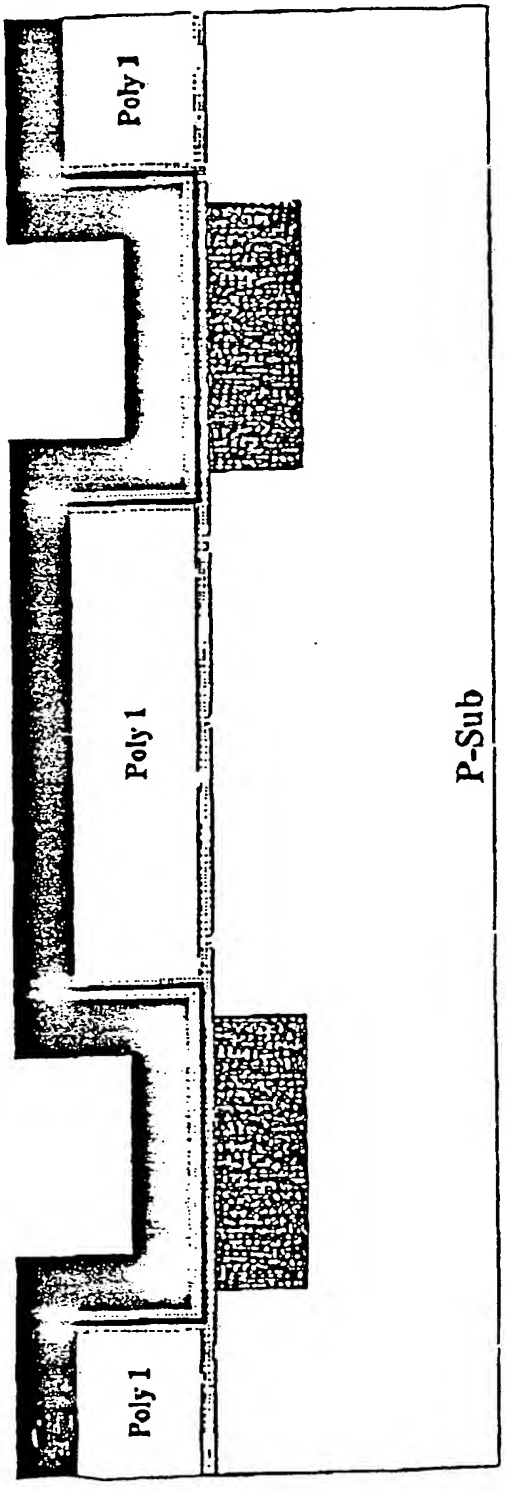


Fig. 4A

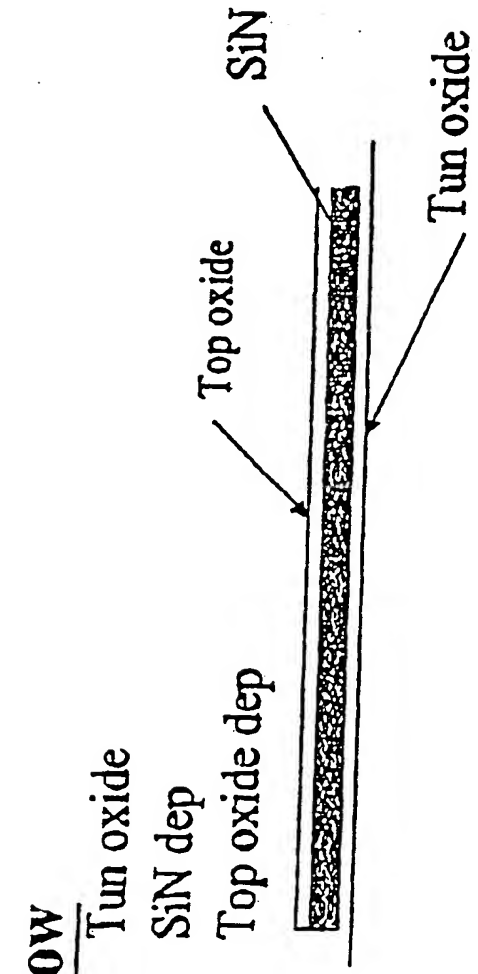


Fig. 4B

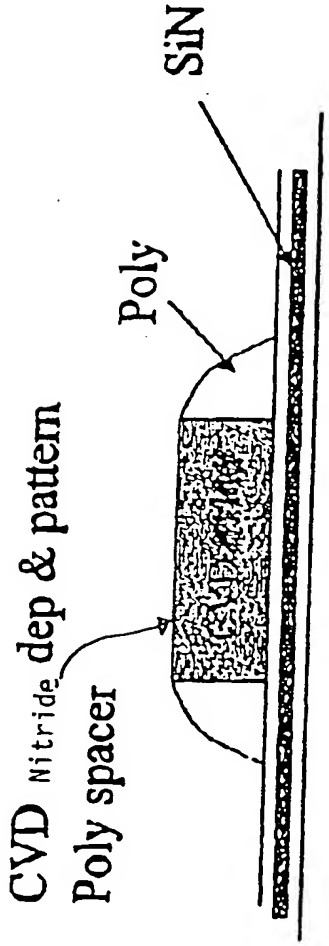


Fig. 4C

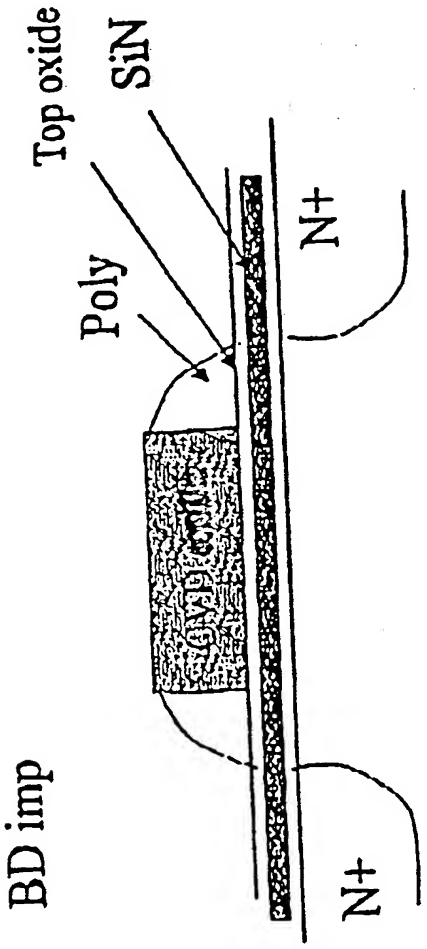
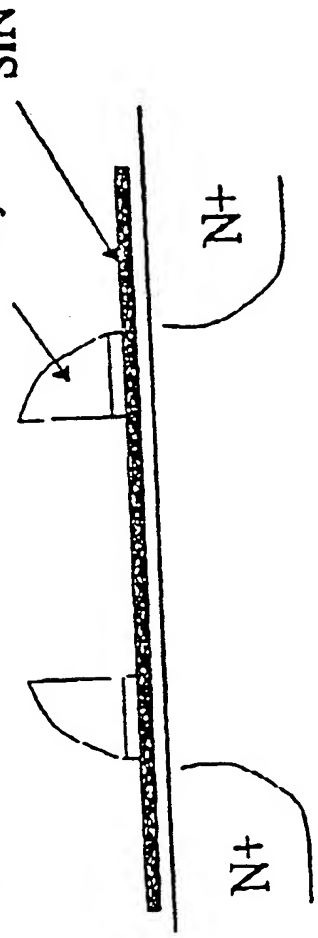


Fig. 4D



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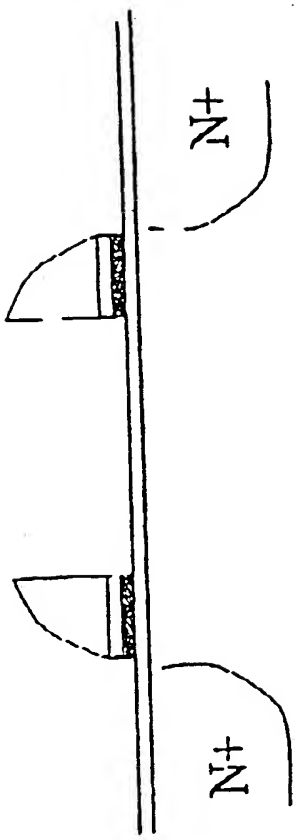

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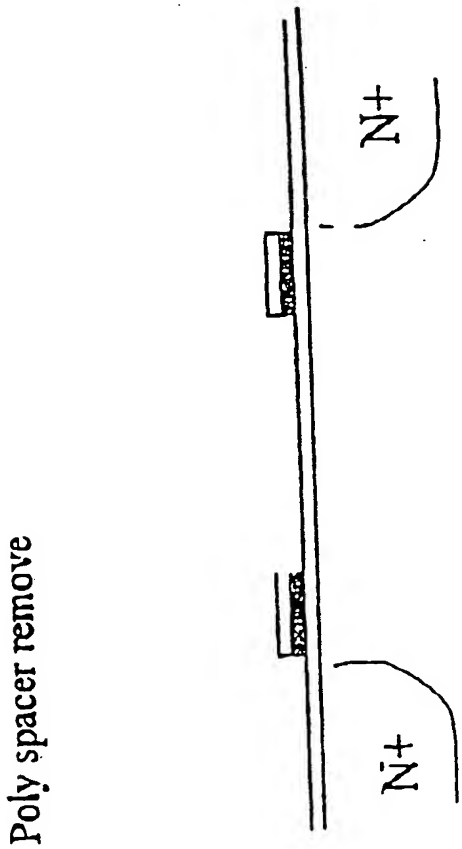

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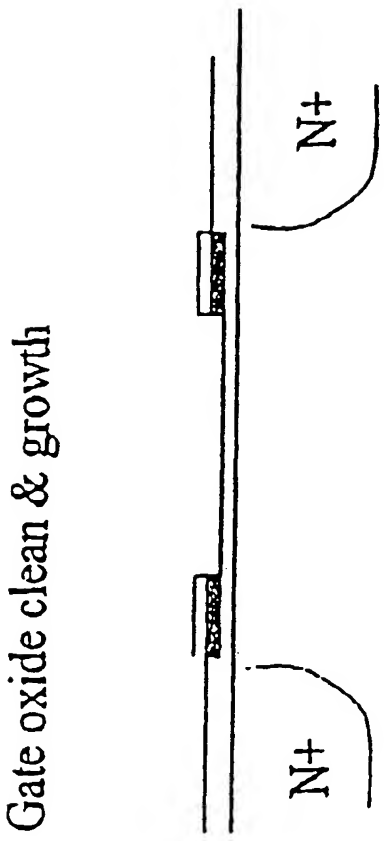
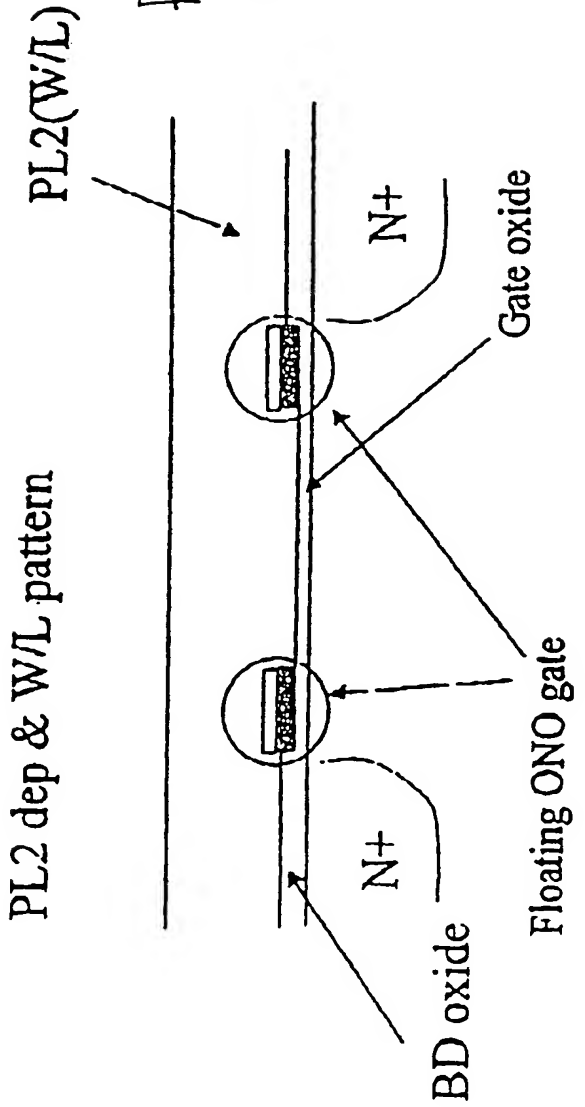

Gate oxide clean & growth
N+
N+

Fig. 4H


PL2 dep & W/L pattern
PL2(W/L)
N+
N+
Gate oxide
Floating ONO gate
BD oxide

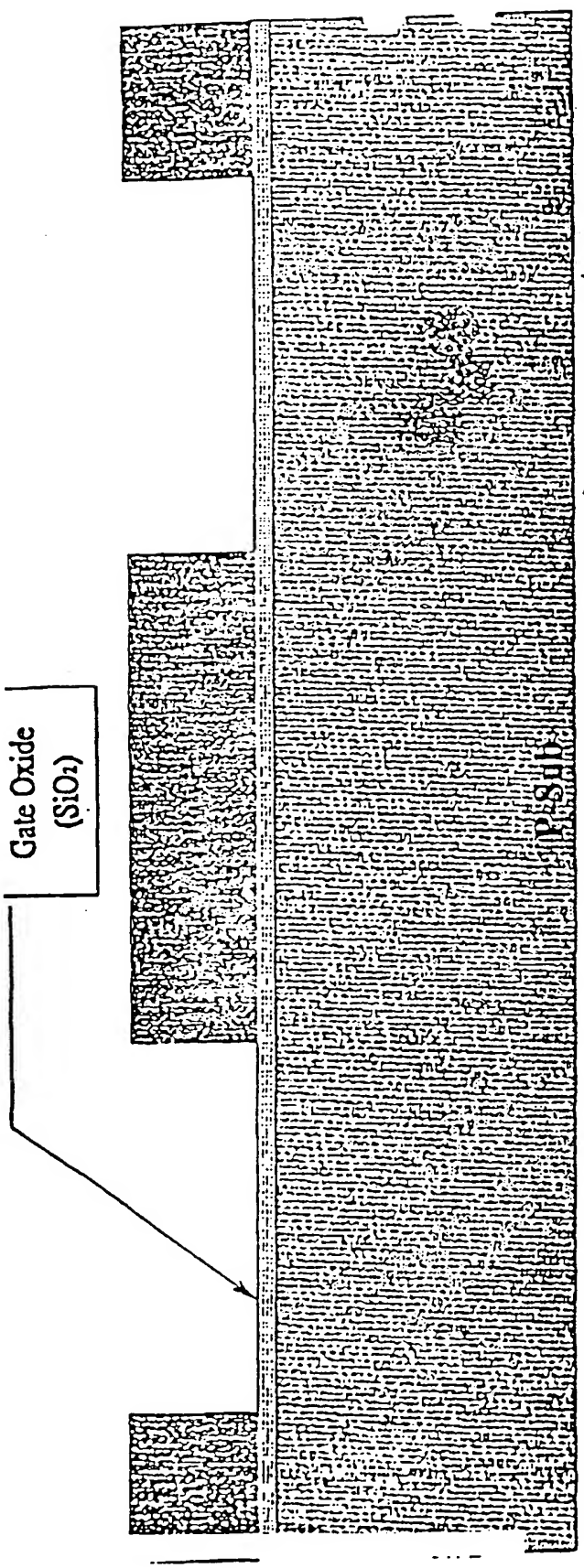


Fig. 5A

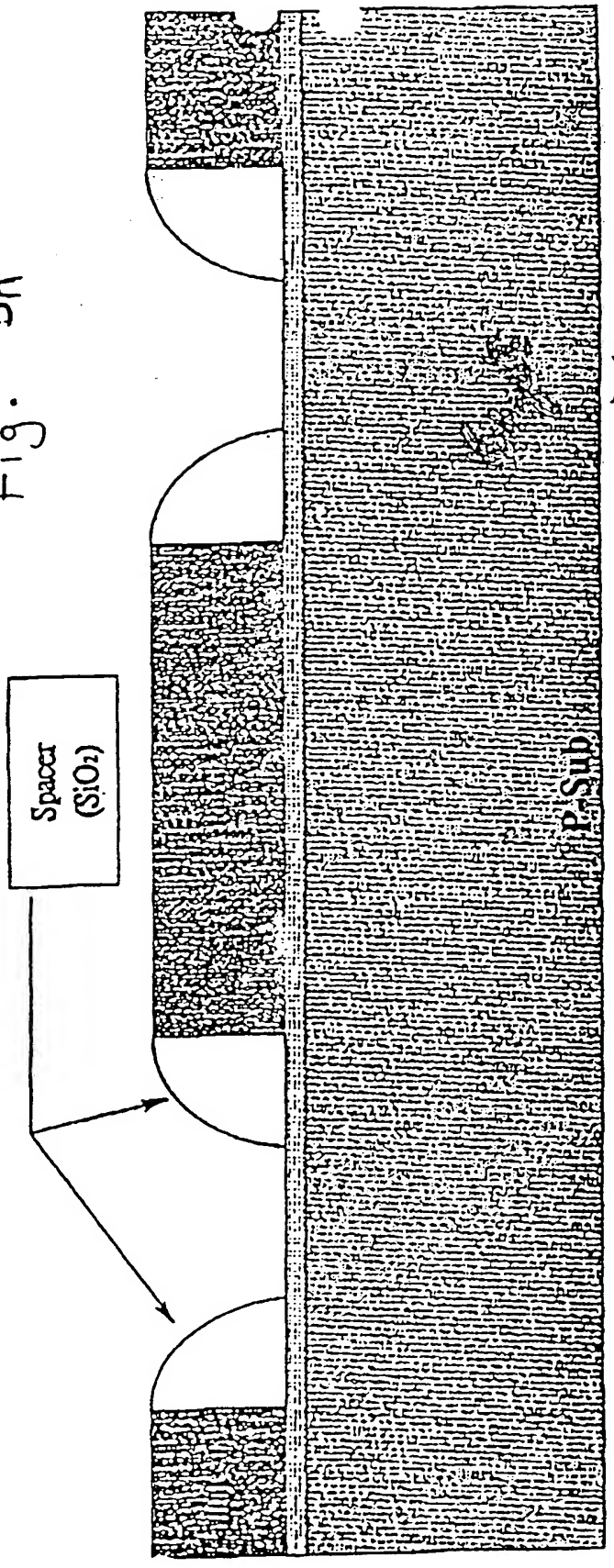


Fig. 5B

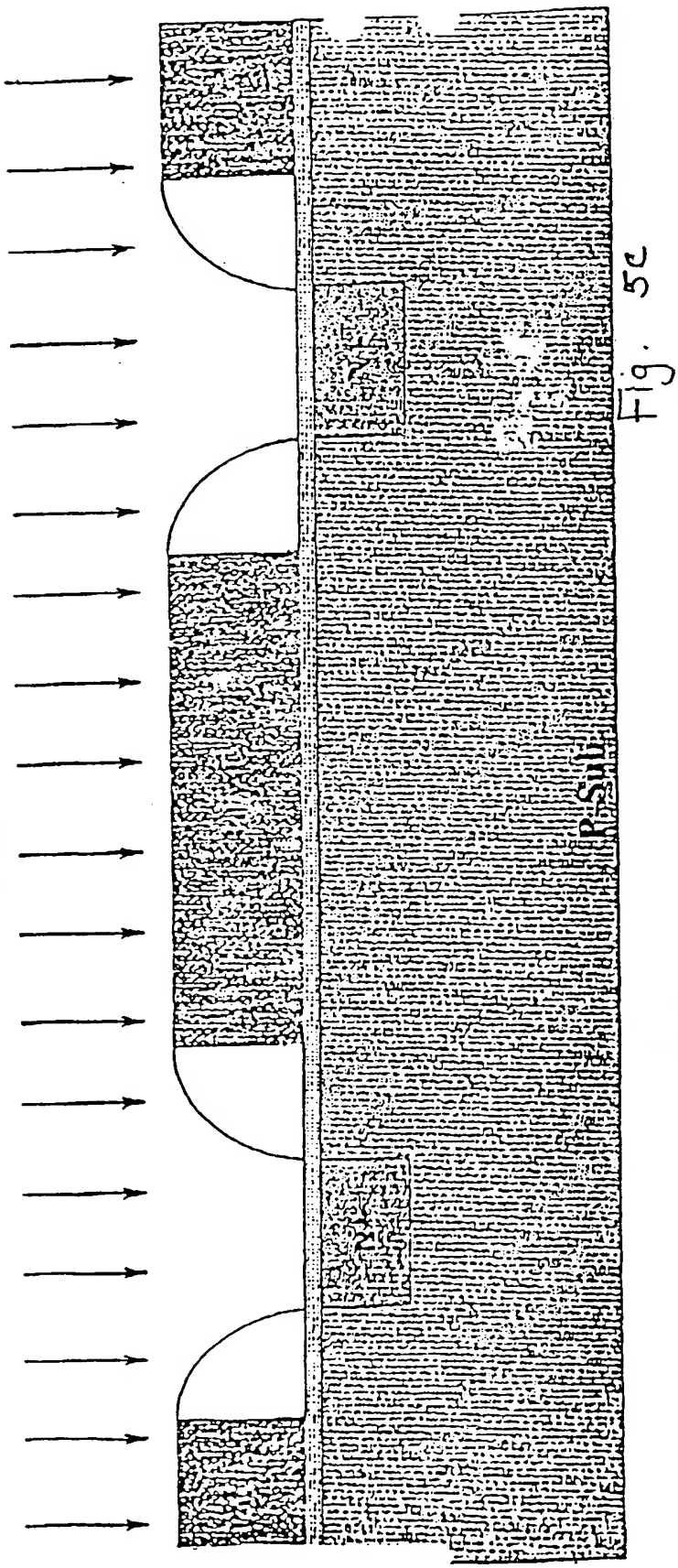


Fig. 5c

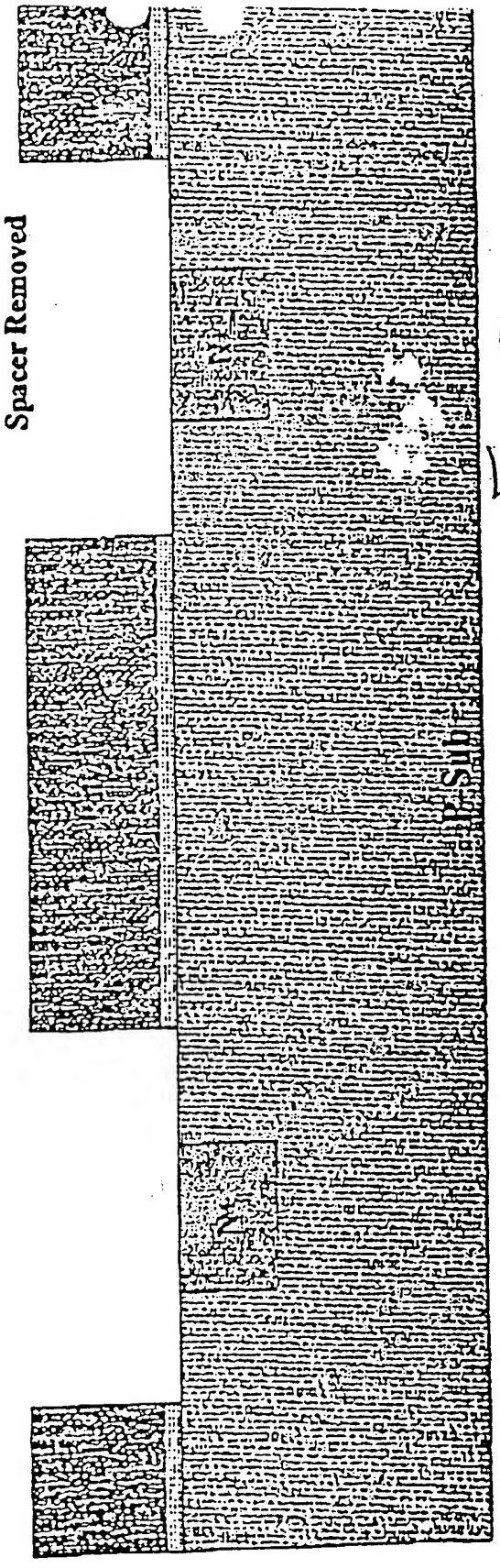


Fig. 5d

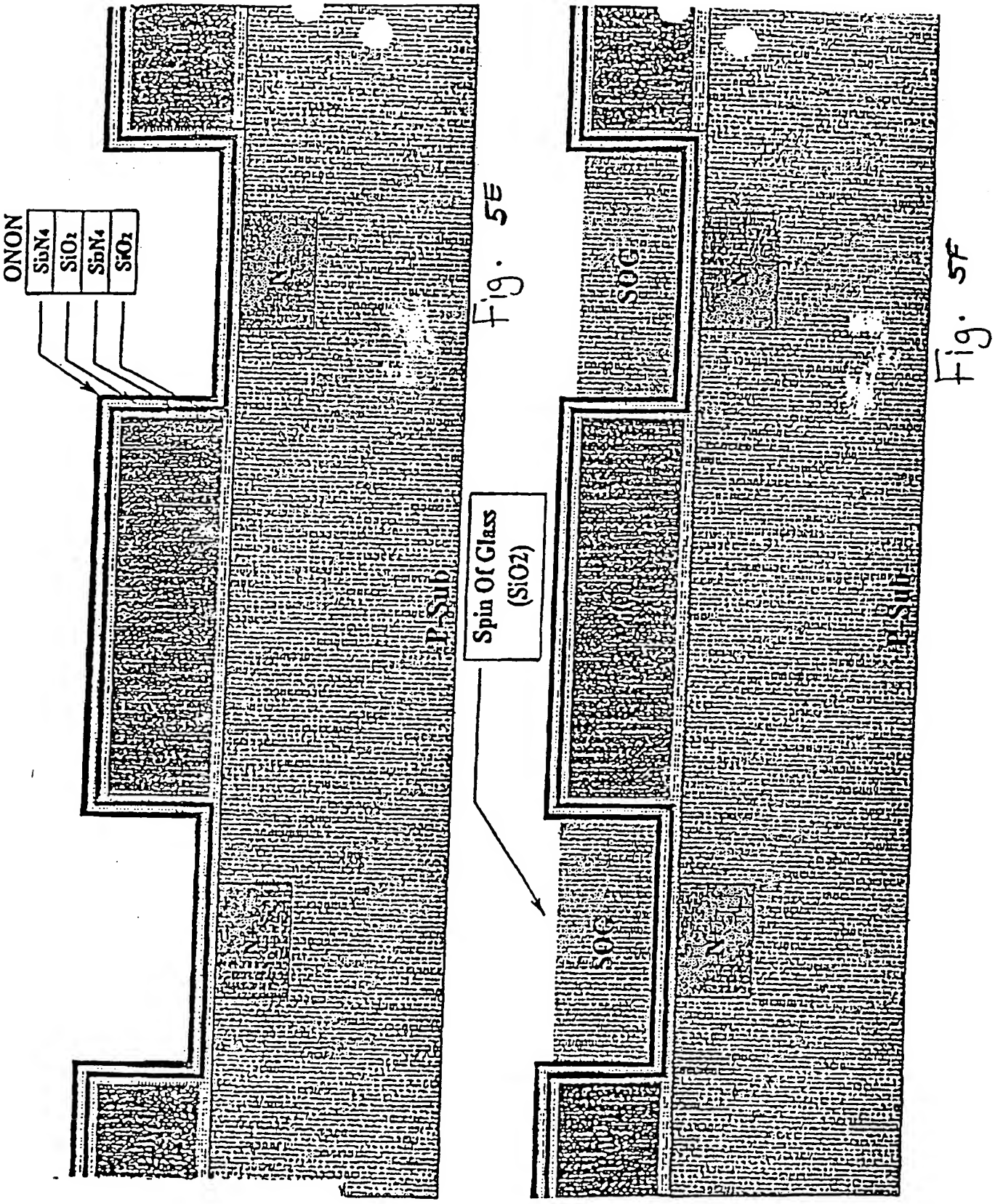


Fig. 5E

Fig. 5F

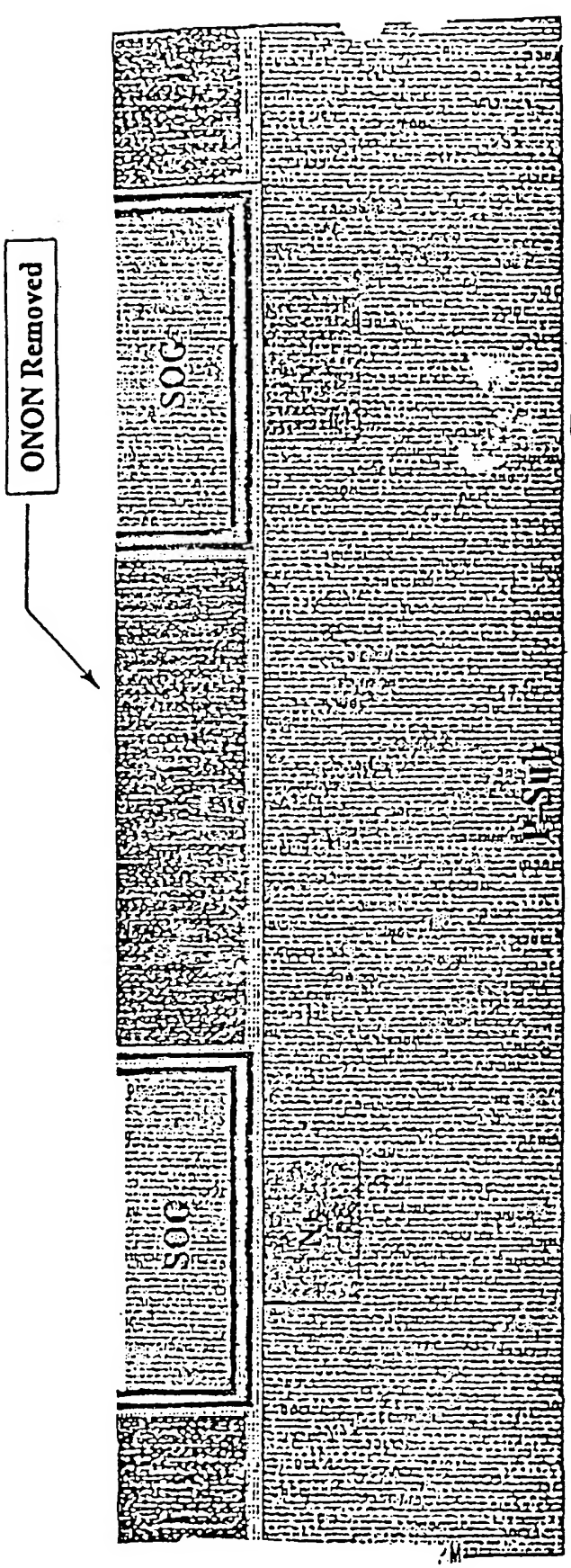


Fig. 5G

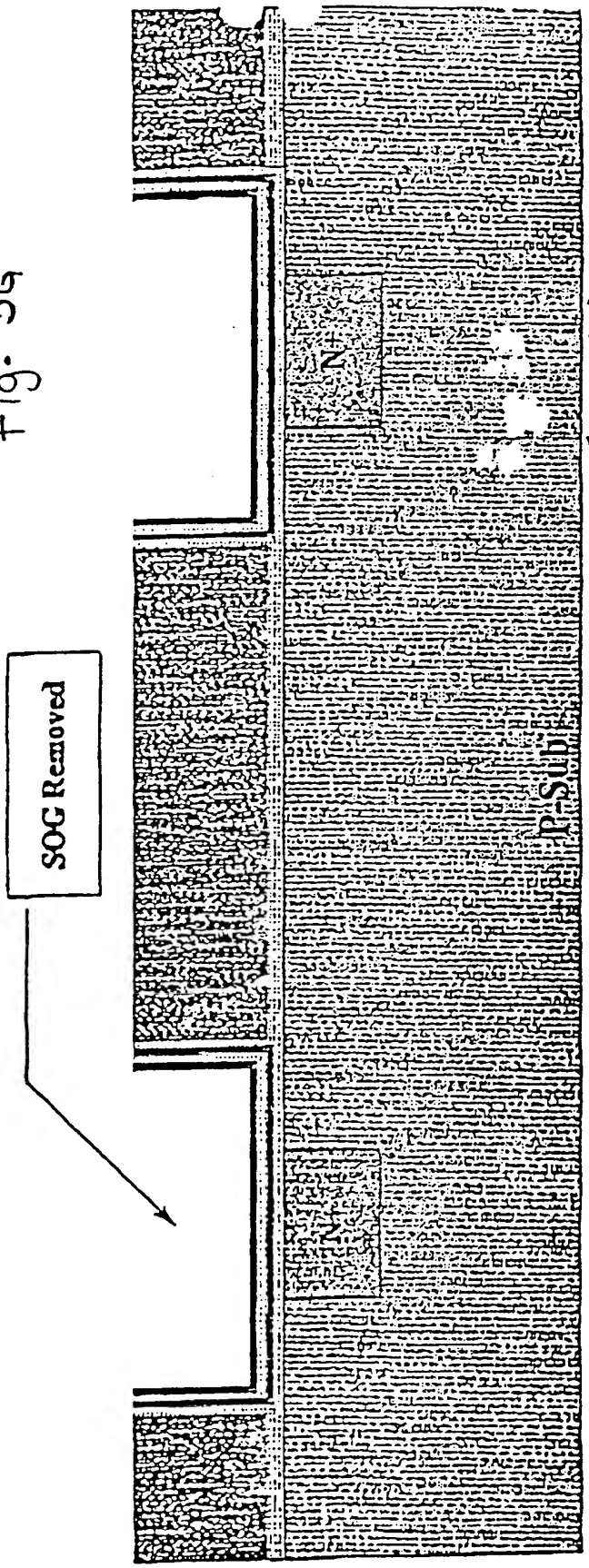


Fig. 5H

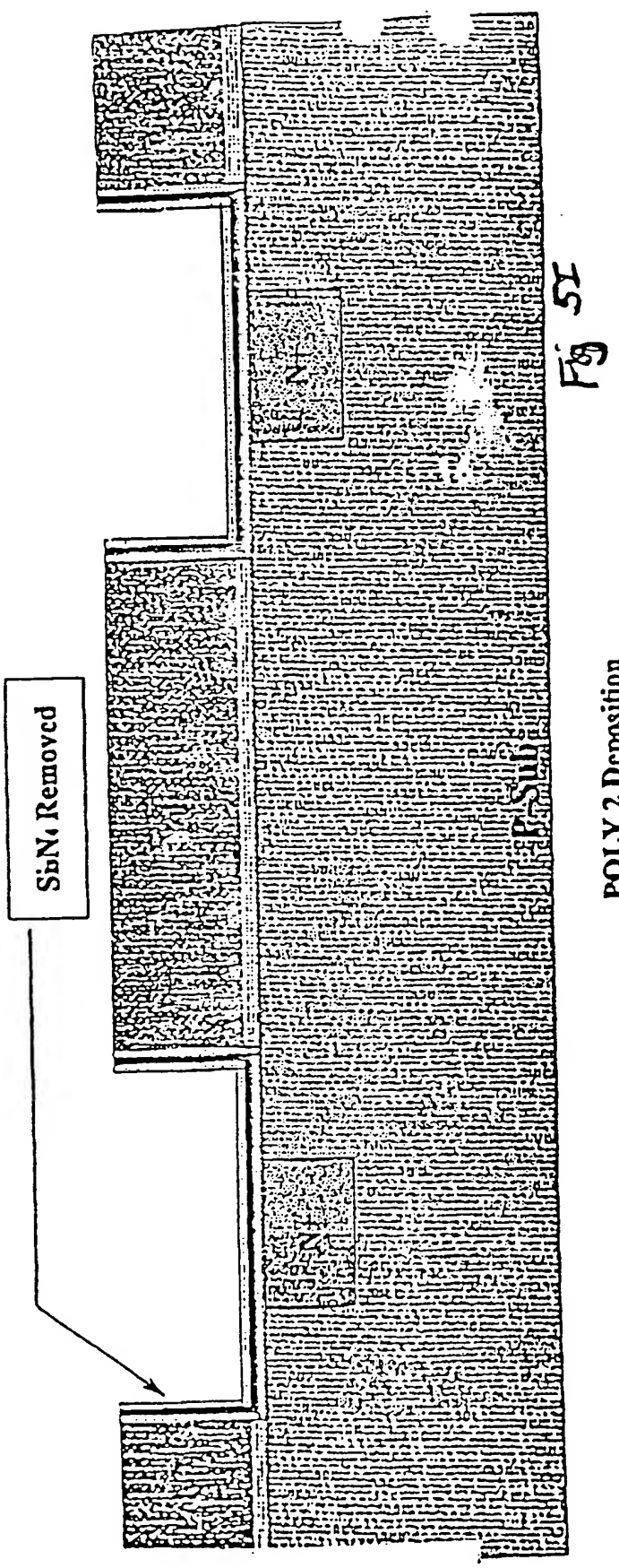


Fig 5E

POLY 2 Deposition

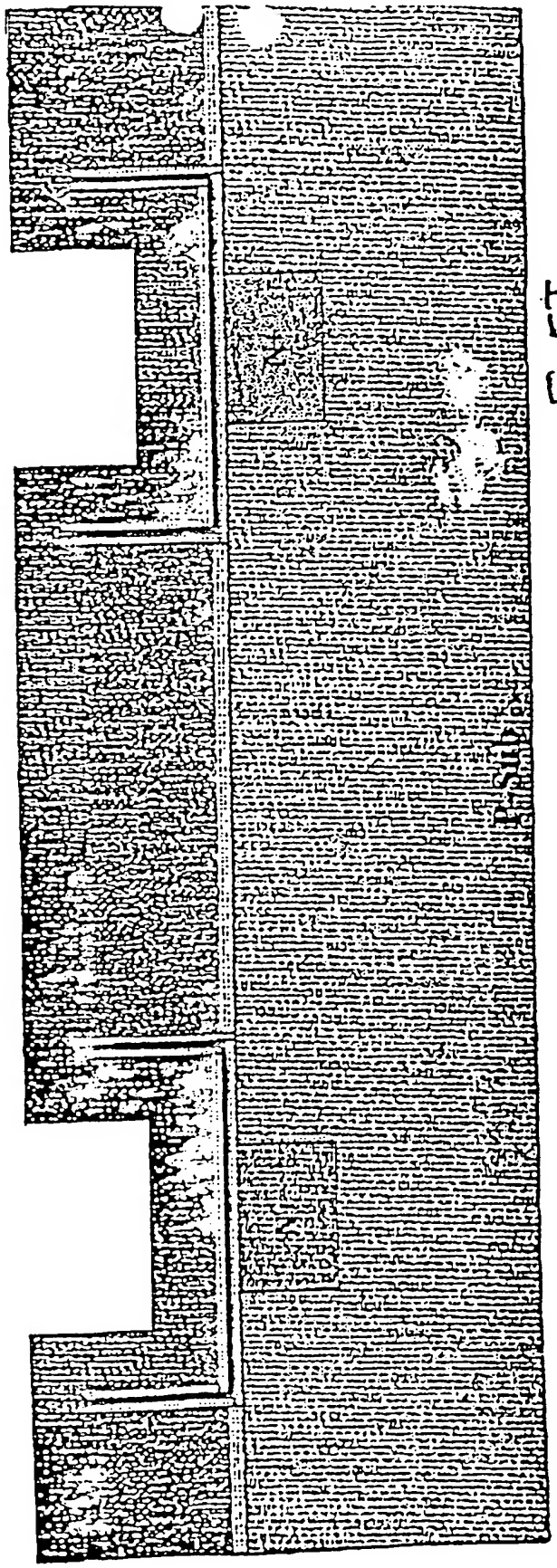


Fig 5F

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/23484

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :H01L 29/788, 29/792
US CL :257/315, 316, 317, 321, 324
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/315, 316, 317, 321, 324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 6,011,725 A (EITAN) 04 January 2000 (04.01.2000), col. 11, lines 20-52.	1-3
A	US 5,929,480 A (HISAMUNE) 27 July 1999 (27.07.1999), see entire document.	4-7
A	US 5,408,115 A (CHANG) 18 April 1995 (18.04.1995), see entire document.	4-7

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"E" earlier document published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
24 OCTOBER 2000

Date of mailing of the international search report
14 NOV 2000

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